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10/676,609	10/02/2003	Susumu Kasukabe	500.43175X00	7923

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EXAMINER	
TANG, MINH NHUT	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,609	KASUKABE ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 8, 15, 18-19 and 23 are objected to because of the following informalities:

a/ in claim 1, line 3, "the wafer" should be -- the wafer part --. Furthermore, the limitations "a pitch between said electrode pads" (line 9), and "a pitch between said contact terminals" (line 10) are vague because it is not clear which electrode pads and contact terminals having a pitch. For examination purposes, "a pitch between said electrode pads", and "a pitch between said contact terminals" are interpreted as -- a pitch between each adjacent electrode pads of said electrode pads --, and -- a pitch between each corresponding adjacent contact terminals of said contact terminals --, respectively.

b/ in claims 8, 18 and 23, likewise claim 1, "a pitch between the/said electrode pads", and "a pitch between said contact terminals" are interpreted as -- a pitch between each adjacent electrode pads of the/said electrode pads --, and -- a pitch between each corresponding adjacent contact terminals of said contact terminals --, respectively.

c/ in claim 15, line 6, "problem" should be -- probe --.

d/ in claim 19, line 3, since the term "can be" makes the claims indefinite therefore, "can both be" should be -- are both --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Mok et al. (U.S.P. 6,799,976).

As to claim 1, Mok et al. discloses, in Fig. 14, a probe sheet (16) comprising contact terminals (61a-61n) arranged in a first surface (62a) of the probe sheet (16) to oppose a wafer part (92, Fig. 13) to contact with electrodes (i.e., I/O pads of the IC 44) provided on the wafer part (92); wirings (15, 66a-66n), each being drawn from one of said contact terminals (61a-61n) in the probe sheet (16); and electrode pads (64a-64n), each being arranged in second surface (62b) of the probe sheet (16) at an opposite side thereof to the first surface (62a) and electrically connected to one of said wirings (15, 66a-66n), wherein a pitch (83) between each adjacent electrode pads of said electrode pads (64a-64n) in the second surface (62b) of the probe sheet (16) is wider than a pitch (20) between each corresponding adjacent contact terminals of said contact terminals (61a-61n) in the first surface (62a) thereof.

As to claim 2, Mok et al. discloses in Fig. 14, said contact terminals (61a-61n) are arranged according to an array of peripheral electrodes (I/O pads) of semiconductor

devices (44) formed on said wafer part (92), and wherein said electrode pads (64a-64n) are arranged in a grid pattern.

As to claim 3, Mok et al. discloses in Fig. 14, a metallic sheet (not shown), from which at least a part corresponding to signal electrode pads of the electrode pads (64a-64n) is removed, is provided on the second surface (62b) of the probe sheet (16).

As to claim 4, Mok et al. discloses in Fig. 14, a linear expansion coefficient of said metallic sheet is equal to a linear expansion coefficient of said wafer part (44).

As to claim 5, Mok et al. discloses in Fig. 14, said metallic sheet is a 42 alloy sheet.

As to claim 6, Mok et al. discloses in Fig. 21, dummy terminals (114), each of which has a larger contact area with the wafer part (92) than that of each of said contact terminal (61a-61n), are provided on the first surface (62a) of the probe sheet (16) on which said contact terminals (61a-61n) are provided.

As to claim 7, Mok et al. discloses in Fig. 14, said contact terminals (61a-61n) are each created by using an anisotropically etched hole in a crystalline substrate as a cast.

As to claim 8, Mok et al. discloses, in Fig. 14, a probe card (60a) comprising a probe sheet (16) having contact terminals (61a-61n) being arranged in a first surface (62a) of the probe sheet (16) to oppose a wafer part (92, Fig. 13) to contact with electrodes (i.e., I/O pads of the IC 44) provided on the wafer part (92), wirings (15, 66a-66n) each being drawn from one of said contact terminals (61a-61n), and electrode pads (64a-64n) each being arranged in a second surface (62b) of the probe sheet (16) at an opposite side thereof to the first surface (62a) and electrically connected to one of

said wirings (15, 66a-66n); and a multi-layer wiring substrate (68) being provided at an opposite side of the probe sheet (16) to the wafer part (92) to face the second surface (62b) thereof, the multi-layer wiring substrate (68) has electrodes (72a-72n) each being electrically connected to one of said contact terminals (61a-61n) through the one of the electrode pads (64a-64n) and formed on a surface (i.e., upper surface) of the multi-layer wiring substrate (68), and wherein a pitch (83) between each adjacent electrode pads of said electrode pads (64a-64n) in the second surface (62b) of the probe sheet (16) is wider than a pitch (20) between each corresponding adjacent contact terminals of said contact terminals (61a-61n) in the first surface (62a) thereof.

As to claim 9, Mok et al. discloses in Fig. 14, said contact terminals (61a-61n) are arranged according to an array of peripheral electrodes (I/O pads) of semiconductor devices (44) formed on said wafer part (92), and wherein the electrodes (72a-72n) of said multi-layer wiring substrate (68) are arranged in a grid pattern in the surface (upper surface) thereof.

As to claim 10, Mok et al. discloses in Fig. 14, the electrodes (72a-72n) of said multi-layer wiring substrate (68) are provided in a device-opposed-area on the surface (upper surface) of said multi-layer wiring substrate (68).

As to claim 11, Mok et al. discloses in Fig. 14, resistors (i.e., resistors of conductive paths 78a-78n) formed in the multi-layer wiring substrate (68) are mounted in a device-opposed area on said multi-layer wiring substrate (68).

As to claim 12, Mok et al. discloses in Fig. 14, the electrode pads (64a-64n) arranged in the second surface (62b) of the probe sheet (16) and the electrodes (72a-

72n) of said multi-layer wiring substrate (68) are electrically connected by a connection part (77a-77n associated with 78a-78n) extended vertically with respect said multi-layer wiring substrate (68).

As to claim 13, Mok et al. discloses in Fig. 14, the electrodes (72a-72n) of said multi-layer wiring substrate (68) are electrically connected to the electrode pads (64a-64n) arranged in the second surface (62b) of the probe sheet (16) via spring probes (also called 64a-64n) disposed therebetween.

As to claim 14, Mok et al. discloses in Fig. 14, said spring probes (64a-64n) are removable.

As to claim 15, Mok et al. discloses in Fig. 14, each of the electrodes (72a-72n) of said multi-layer wiring substrate (68) and each of the electrode pads (64a-64n) arranged in the second surface (62b) of the probe sheet (16) are electrically connected to each other via a wire (77a-77n associated with 78a-78n) extended therebetween.

As to claim 16, Mok et al. discloses in Fig. 14, said probe card (60a) has a temperature adjustment function.

As to claims 17 and 20, Mok et al. discloses in column 11, lines 1-7, said contact terminals (61a-61n) are each a pyramid-shaped or truncated-pyramid-shaped terminal created by using an anisotropically etched hole in a crystalline substrate as a cast/a shape former.

As to claim 18, Mok et al. discloses, in Fig. 14, a semiconductor test equipment comprising a stage (not shown) on which a wafer part (92) is mounted; and a probe card (60a) having contact terminal (61a-61n) that get in contact with electrodes (i.e., I/O

pads) of semiconductor devices (44) formed on the wafer part (92) and electrically connected to a tester (76) that tests electrical characteristics of the semiconductor devices (44), wherein said probe card (60a) comprises a probe sheet (16) having the contact terminals (61a-61n) being arranged in a first surface (62a) of the probe sheet (16) opposite to the wafer part (92), wirings (15, 66a-66n) each being drawn from one of the contact terminals (61a-61n), and electrode pads (64a-64n) each being arranged in a second surface (62b) of the probe sheet (16) at an opposite side thereof to the first surface (62a) and electrically connection to one of said wirings (15, 66a-66n); and a multi-layer wiring substrate (68) whose electrodes (72a-72n) electrically connected to the contact terminals (61a-61n) via the electrode pads (64a-64n) respectively are provided on a surface opposed to the wafer part (92) across the probe sheet (16), and wherein a pitch (83) between each adjacent electrode pads of the electrode pads (64a-64n) in the second surface (62b) of the probe sheet (16) is wider than a pitch (20) between each corresponding adjacent contact terminals of said contact terminals (61a-61n).

As to claim 19, Mok et al. discloses in Fig. 14, a temperature of the stage and the probe card (60a) and are both controlled.

As to claims 21 and 22, Mok et al. discloses in Fig. 14, the device-opposed area is an area of the multi-layer wiring substrate (68) opposite to semiconductor devices (44) formed on the surface of the wafer part (92) across the probe sheet (16), and that resistors (i.e., resistors of conductive paths 78a-78n) formed in the multi-layer wiring

substrate (68) are mounted on a surface of the multi-layer wiring substrate (68) at an opposite side thereof to the wafer part (92).

As to claim 23, Mok et al. discloses, in Fig. 14, a probe sheet (16) comprising contact terminals (61a-61n) arranged in a first surface (62a) of the probe sheet (16) to oppose a wafer part (92, Fig. 13) to contact with electrodes (i.e., I/O pads of the IC 44) provided on the wafer part (92); wirings (15, 66a-66n), each being drawn from one of said contact terminals (61a-61n) in the probe sheet (16); and electrode pads (64a-64n), each being arranged in second surface (62b) of the probe sheet (16) at an opposite side thereof to the first surface (62a) and electrically connected to one of said wirings (15, 66a-66n), wherein a pitch (83) between each adjacent electrode pads of said electrode pads (64a-64n) in the second surface (62b) of the probe sheet (16) is wider than a pitch (20) between each corresponding adjacent contact terminals of said contact terminals (61a-61n) in the first surface (62a) thereof, and wherein ones of said electrode pads (64a-64n) extending in a direction away from an area of the contact terminals (61a-61n) are laid out in an array having at least three rows extending at least somewhat parallel to the area.

As to claim 24, Mok et al. discloses in Fig. 14, the electrode pads (64a-64n) of a subject row of the rows, are staggered with respect to the electrode pads (64a-64n) of a neighboring row.

As to claim 25, Mok et al. discloses in Fig. 14, the wirings (15, 66a-66n) are serpentine wirings, and ones of the serpentine wirings trace serpentine paths between the electrode pads (64a-64n)

As to claim 26, a pitch between ones of the serpentine wirings varies extending in the direction away from the area of the contact terminals (61a-61n).

Response to Arguments

4. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh Tang

MINH NHUT TANG
PRIMARY EXAMINER
5/27/05